

FIG. 4

PRIOR ART

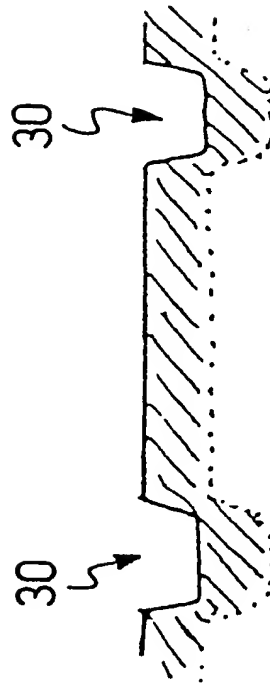


FIG. 5

PRIOR ART

FIG. 6 is a schematic diagram of a memory array structure, showing a cross-section of a memory cell. The diagram illustrates the arrangement of various layers and components, including a word line (WL), bit line (BL), and gate (CG). The structure is shown in a perspective view, with a horizontal axis labeled 'X' and a vertical axis labeled 'Y'. The diagram is labeled 'FIG. 6' in the bottom right corner.

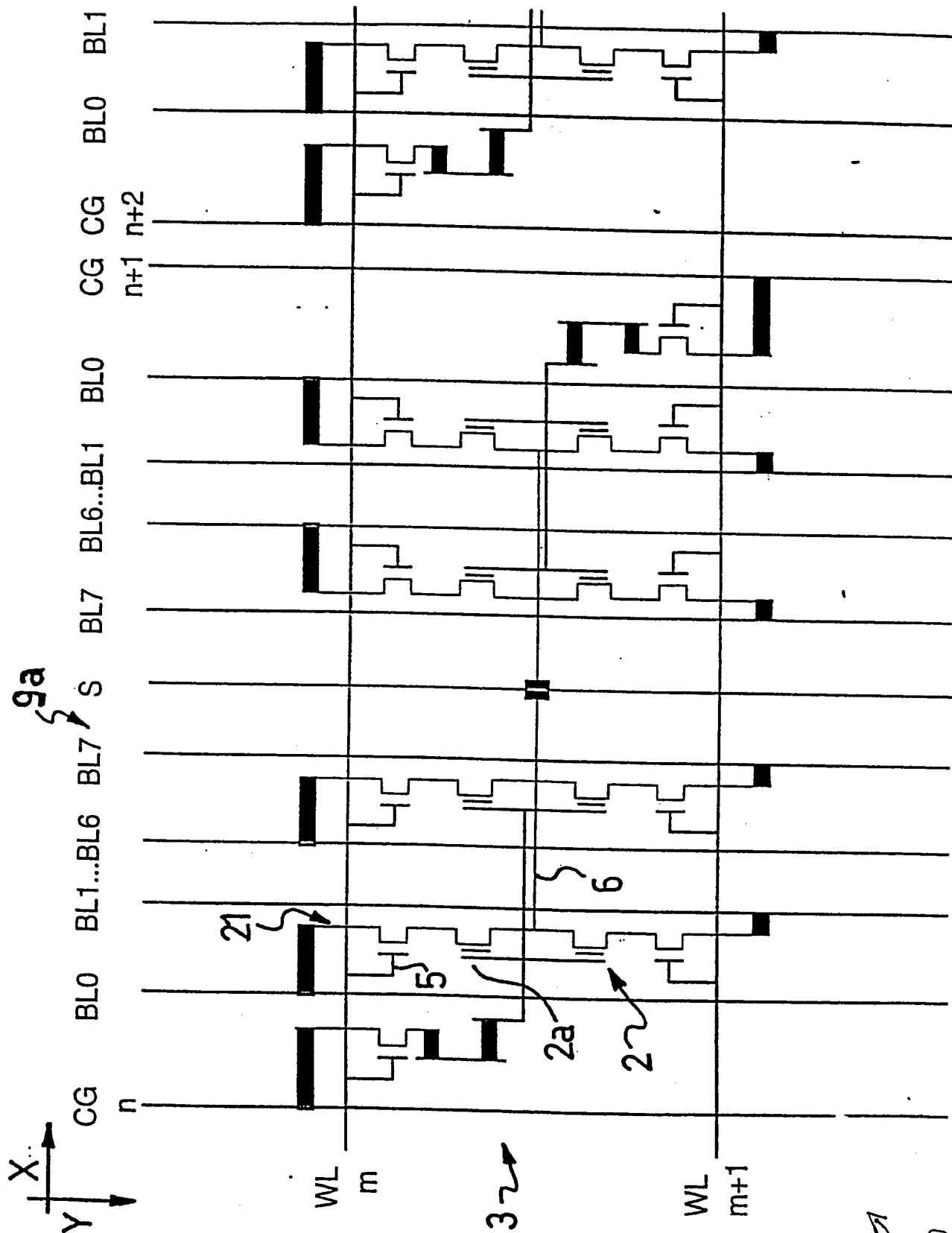


FIG. 6

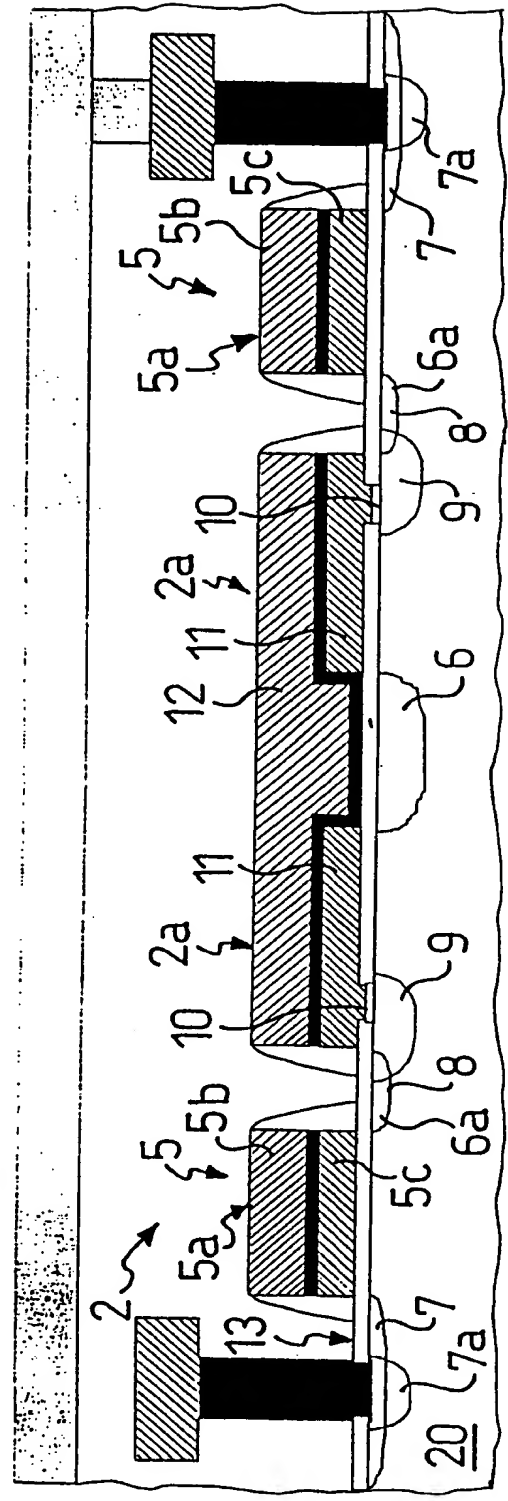
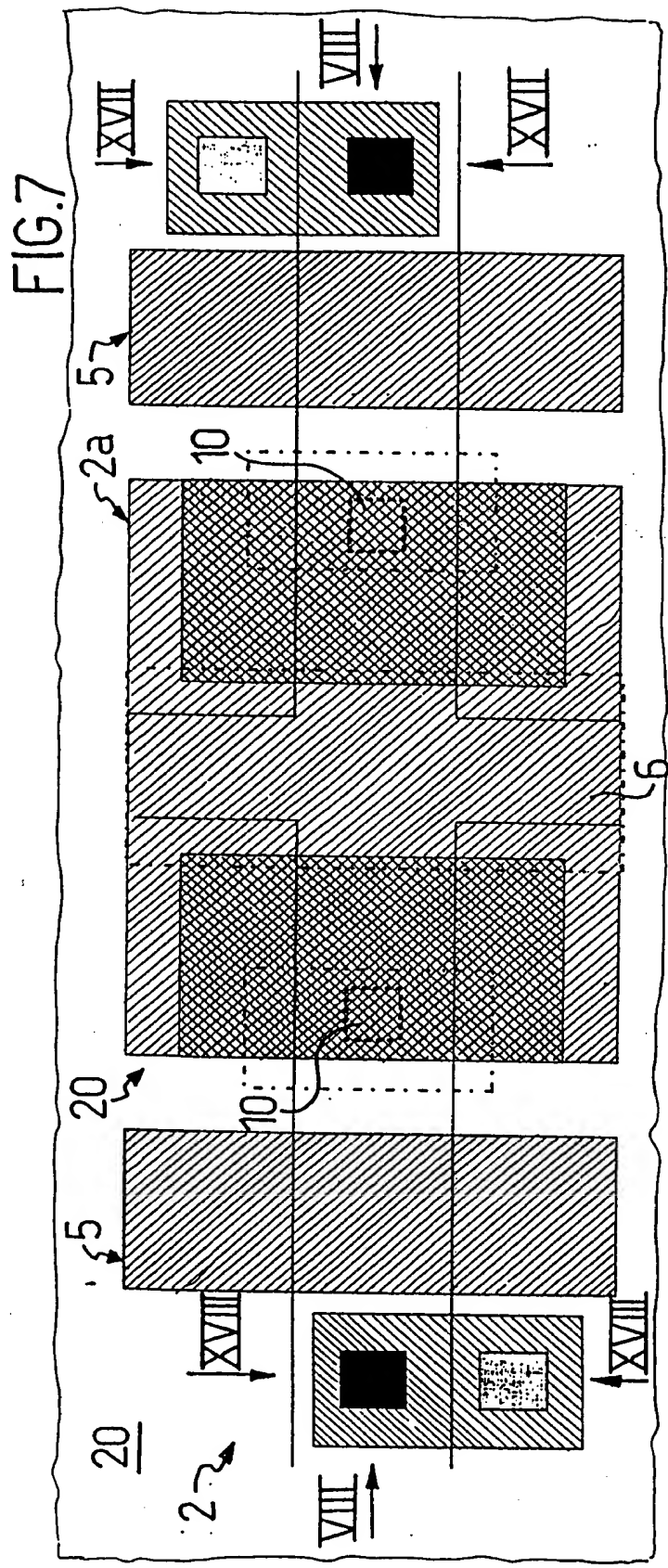


FIG. 8

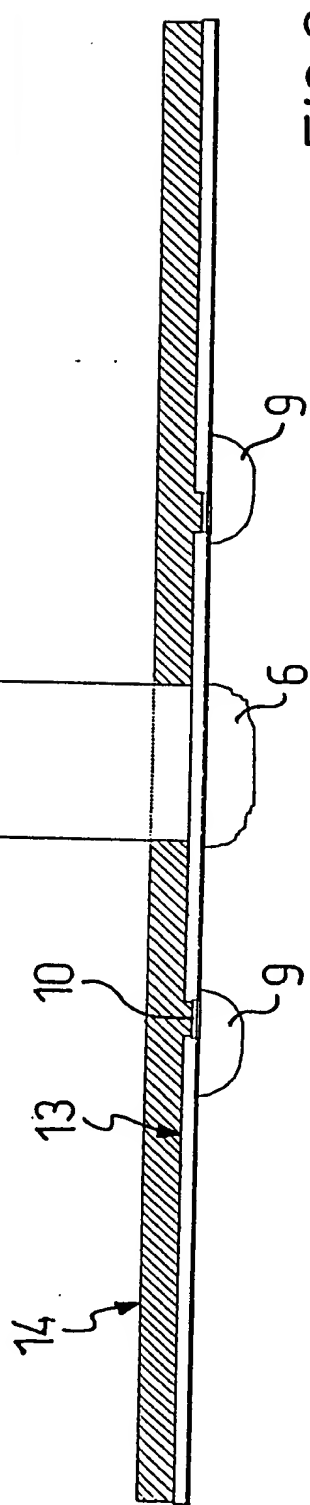


FIG. 9

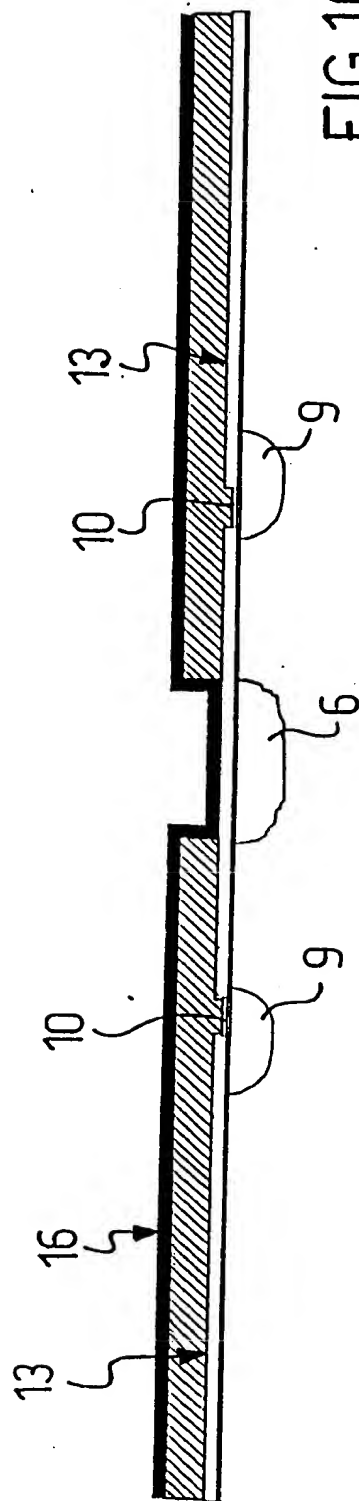


FIG. 10

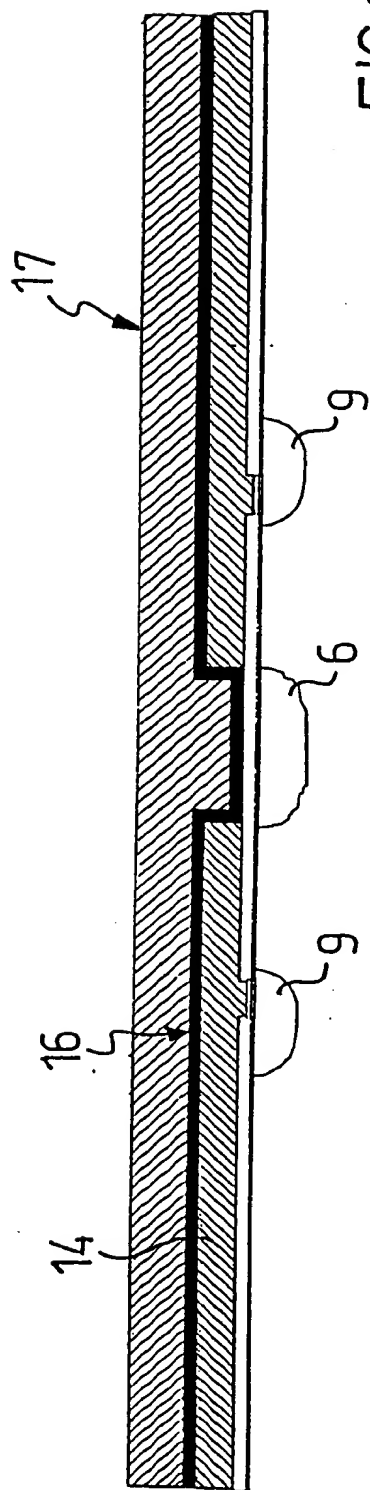


FIG. 11

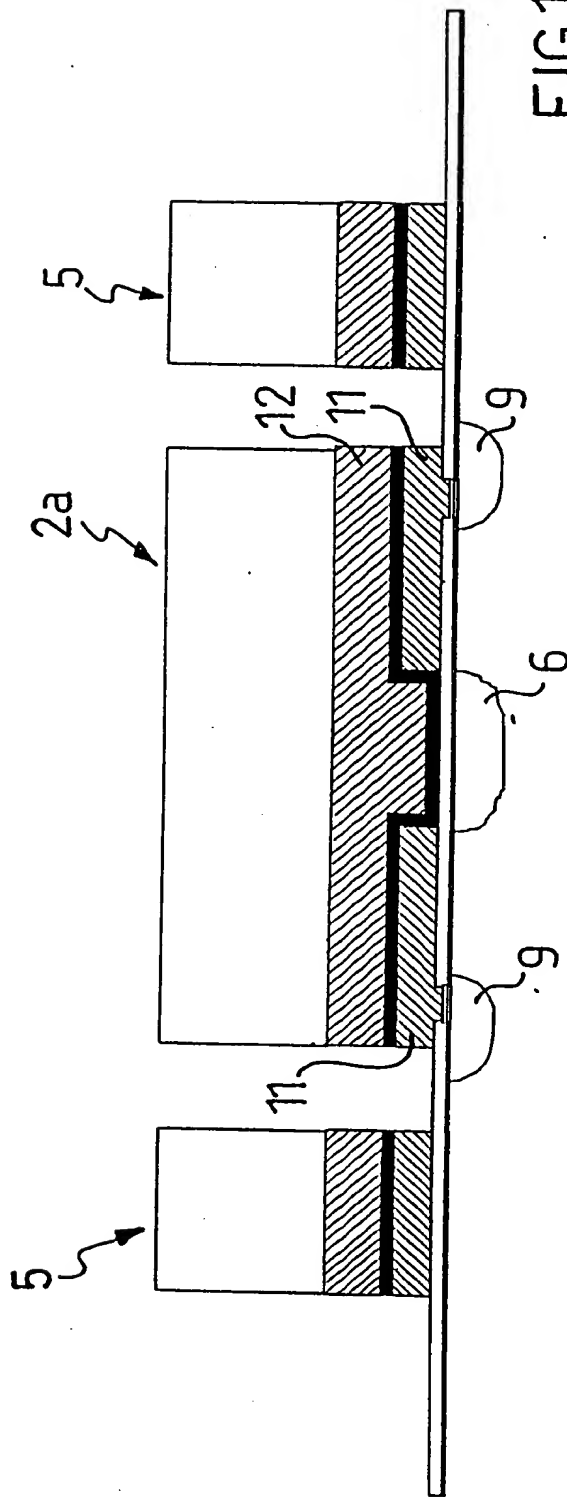
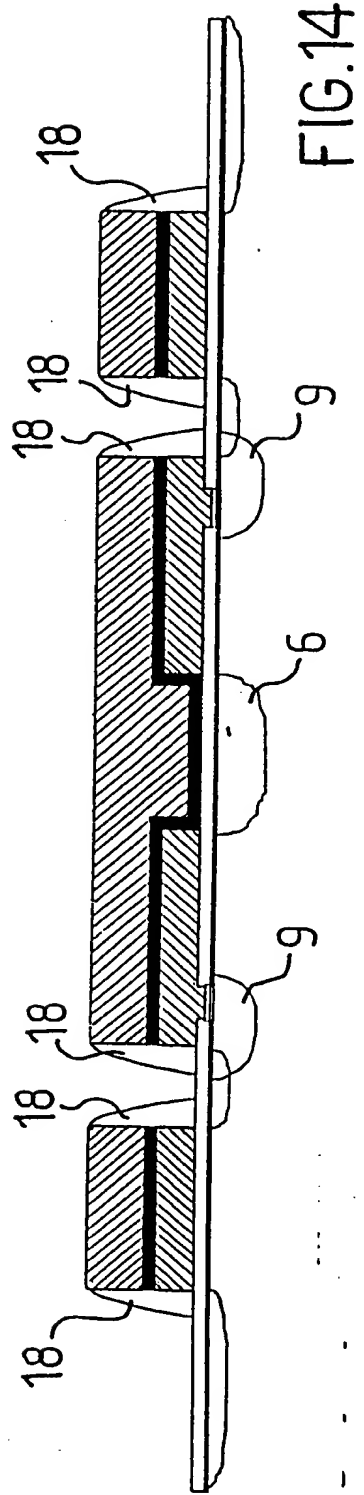
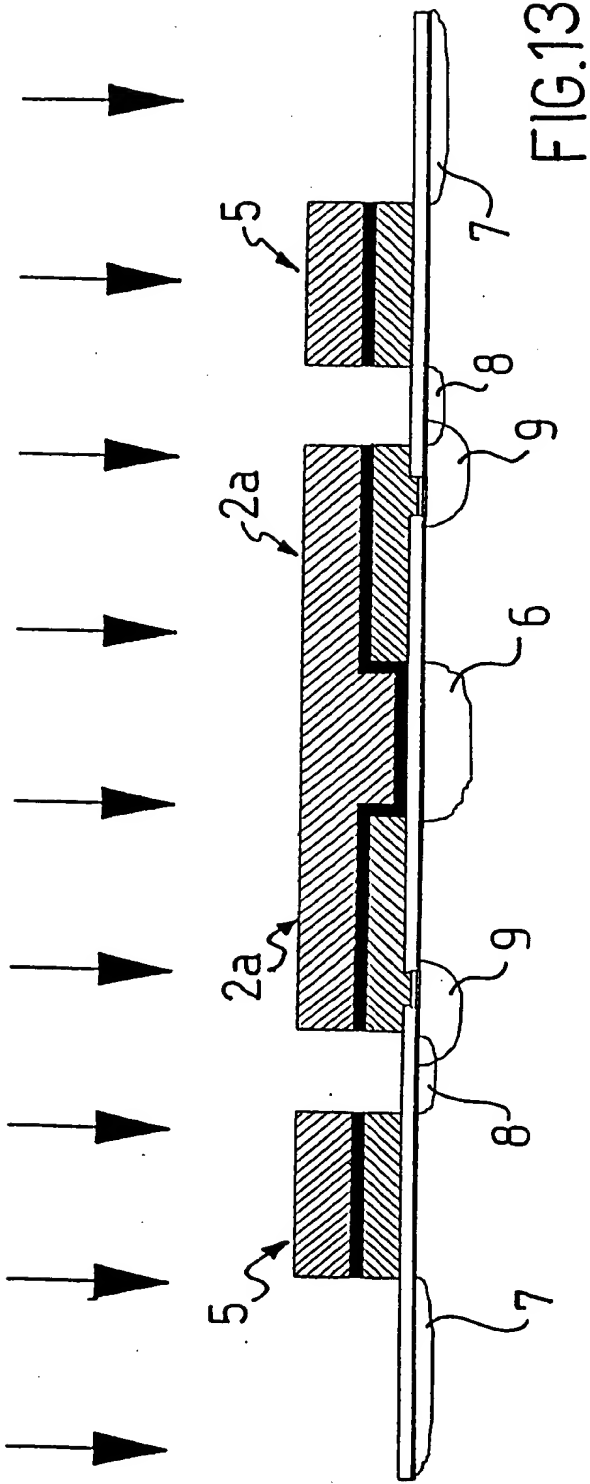


FIG. 12





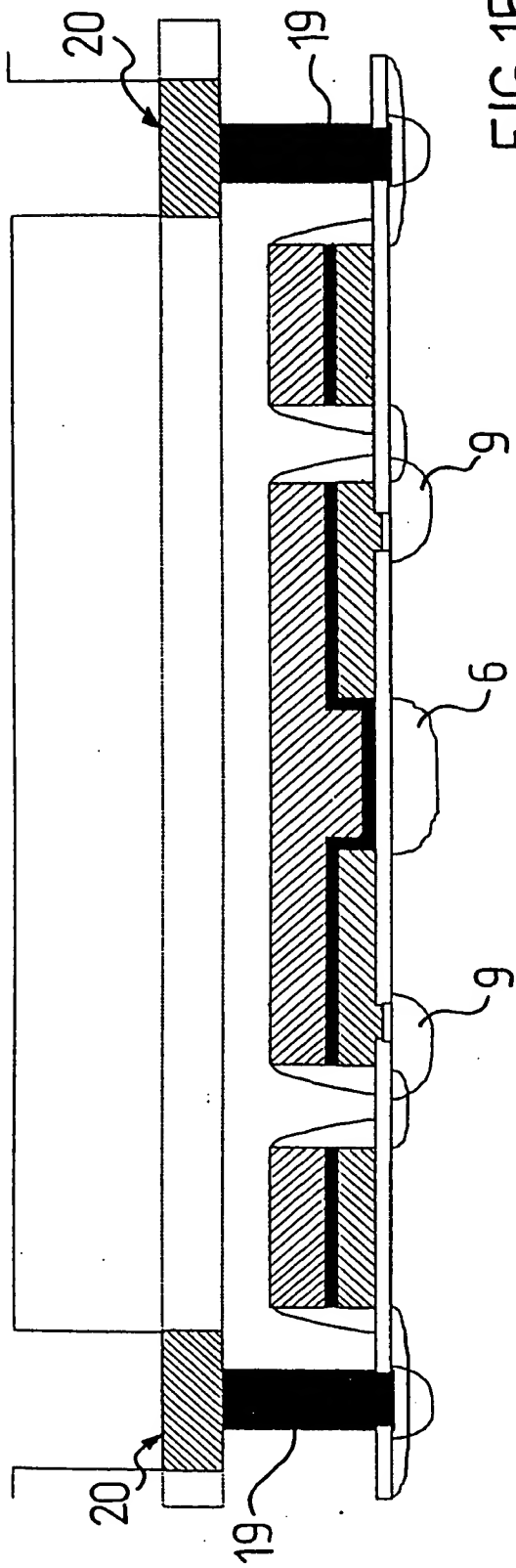


FIG. 15

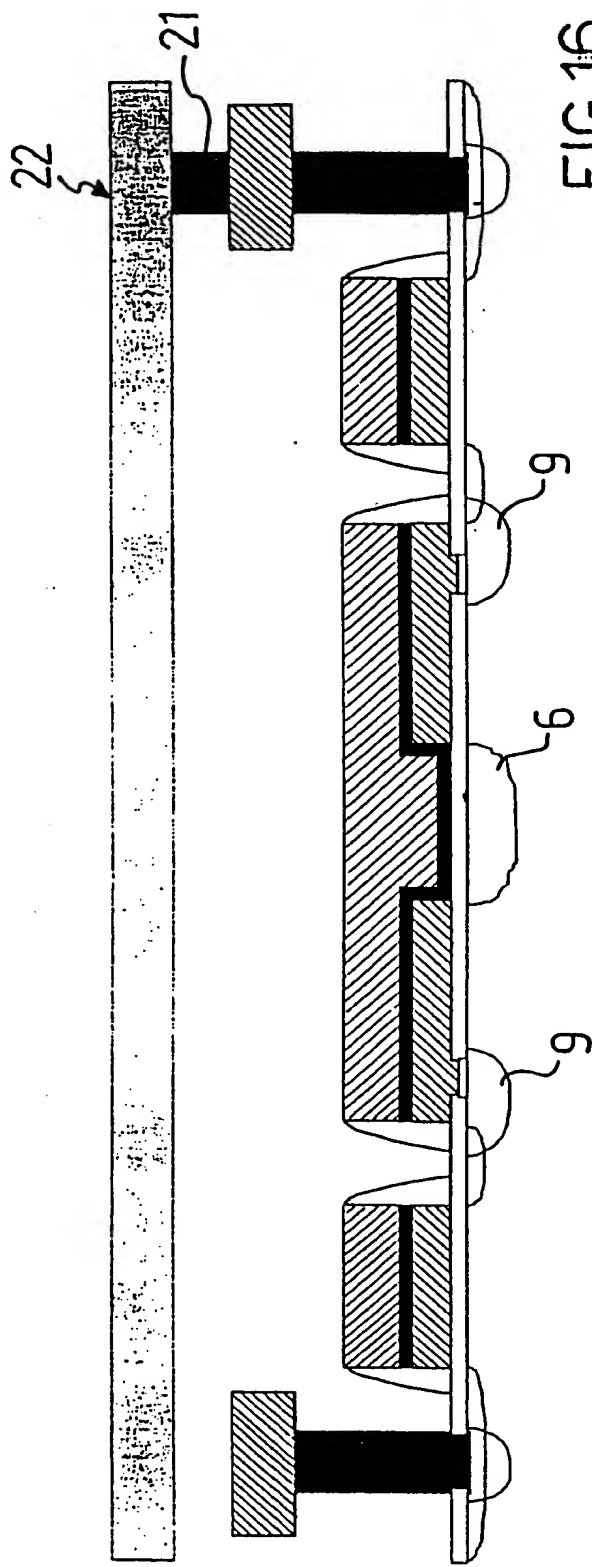


FIG. 16

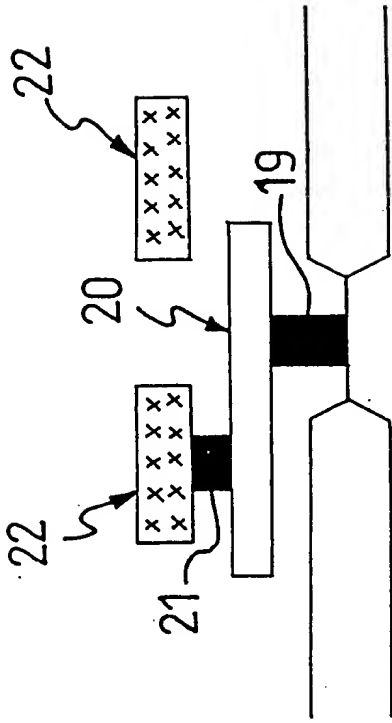


FIG. 17

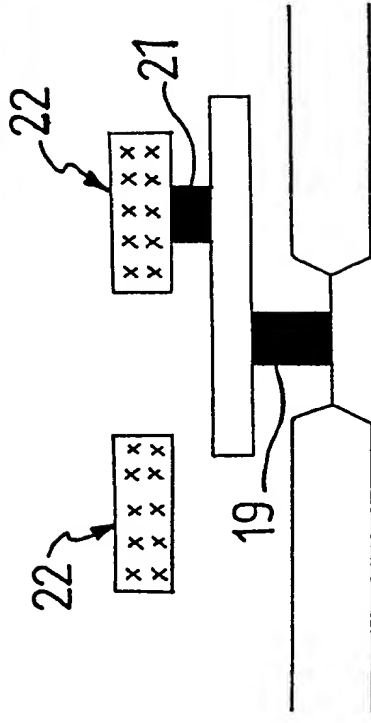


FIG. 18

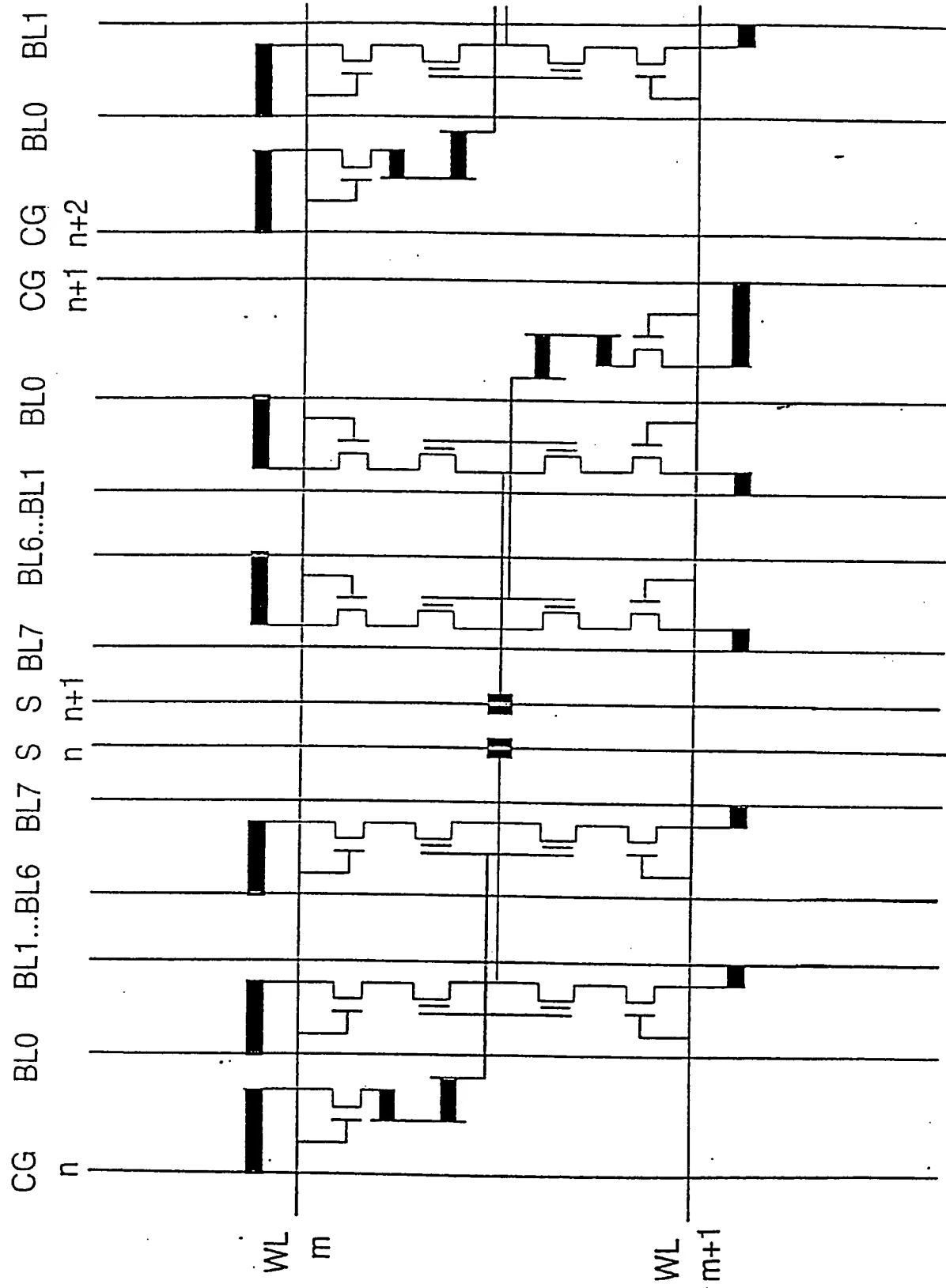


FIG.19

9b

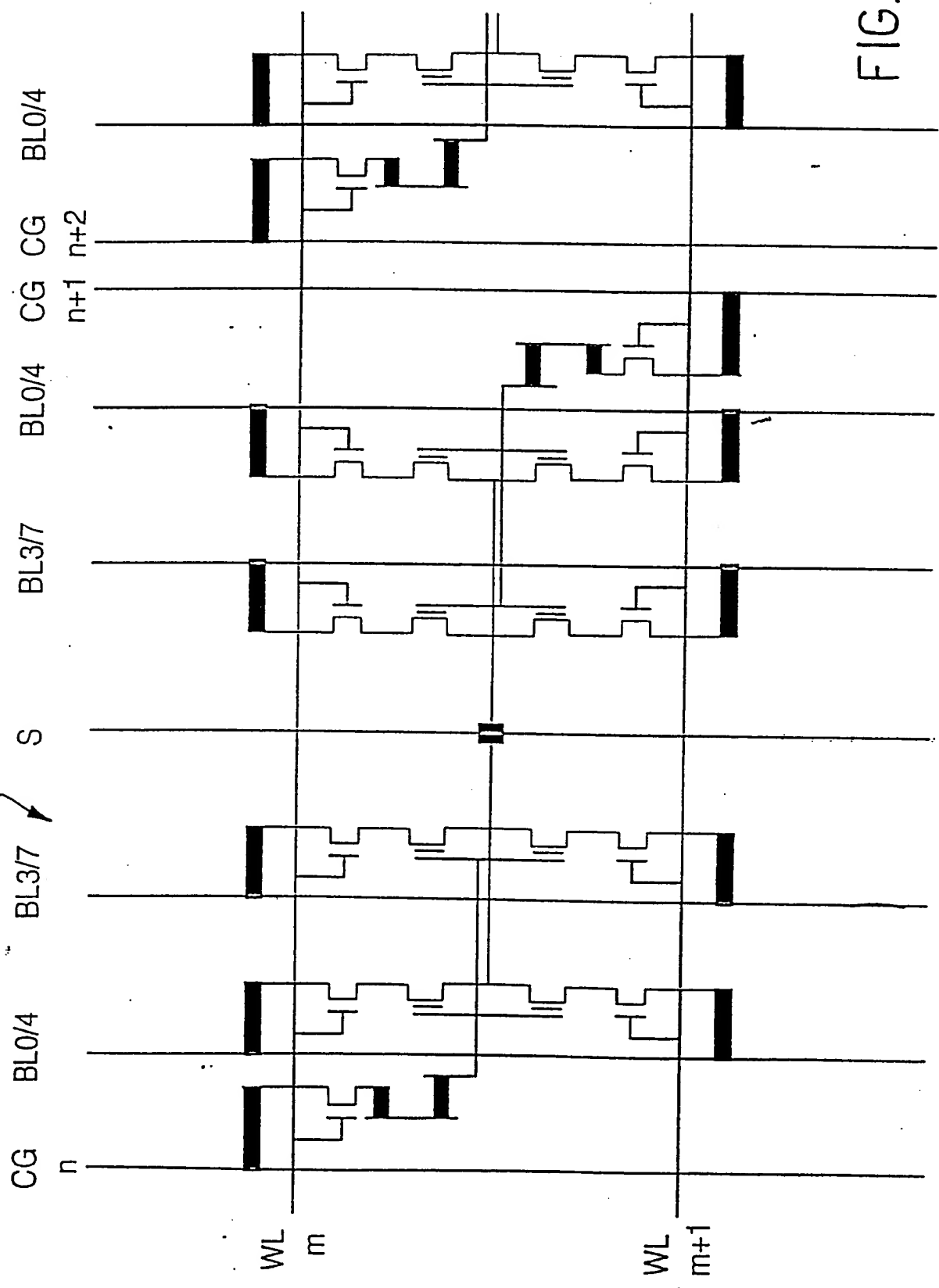


FIG.20